

FIG. 1

1/5

AUS9-2001-0128-US1

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The diagram illustrates the architecture of the FIR 20, divided into two main sections by a dashed line. The top section contains three FIR modules: FIR 12a, FIR 14a, and FIR 15a. FIR 12a outputs OF_{s1}, which feeds into EI_s. FIR 14a outputs OF_{s2} (feeding EI_s), ED_{s2}, and ED_{s1}. FIR 15a outputs OF_{s3} (feeding EI_s) and ED_{s3}. EI_s feeds into the ERROR HANDLER MODULE 21. ED_{s2}, ED_{s1}, and ED_{s3} feed into the PROCESSOR RUNTIME DIAGNOSTIC MODULE 22. The ERROR HANDLER MODULE 21 outputs EC_{s2} to the SCAN DUMP MODULE 23 and ID_s to the PROCESSOR RUNTIME DIAGNOSTIC MODULE 22. The PROCESSOR RUNTIME DIAGNOSTIC MODULE 22 outputs EC_{s1} to the ERROR HANDLER MODULE 21 and ID_s to the SCAN DUMP MODULE 23. The SCAN DUMP MODULE 23 outputs SD_s to the PROCESSOR RUNTIME DIAGNOSTIC MODULE 22. The PROCESSOR RUNTIME DIAGNOSTIC MODULE 22 also outputs to the USER INTERFACE 24. The USER INTERFACE 24 is connected to the bottom section of the diagram, which contains the FIR 20 module, via ID_s.

AUS9-2001-0128-US1

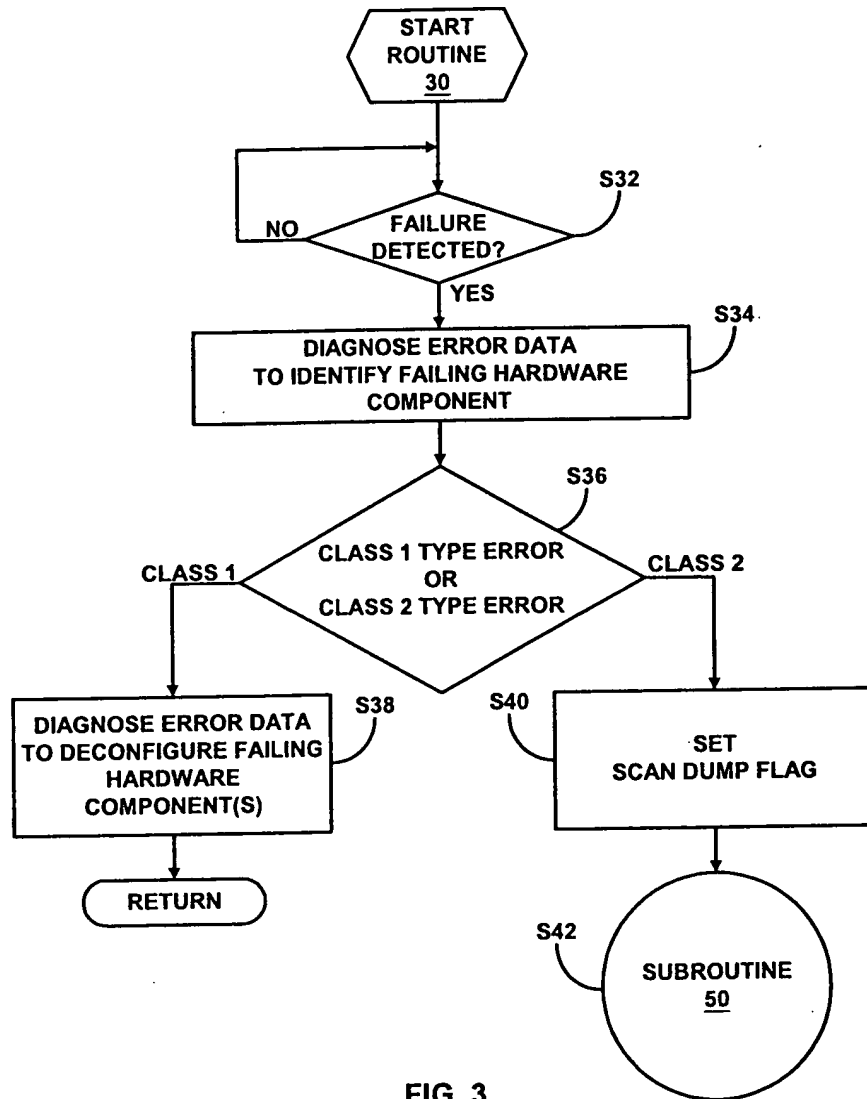


FIG. 3
3/5
AUS9-2001-0128-US1

FIG. 4

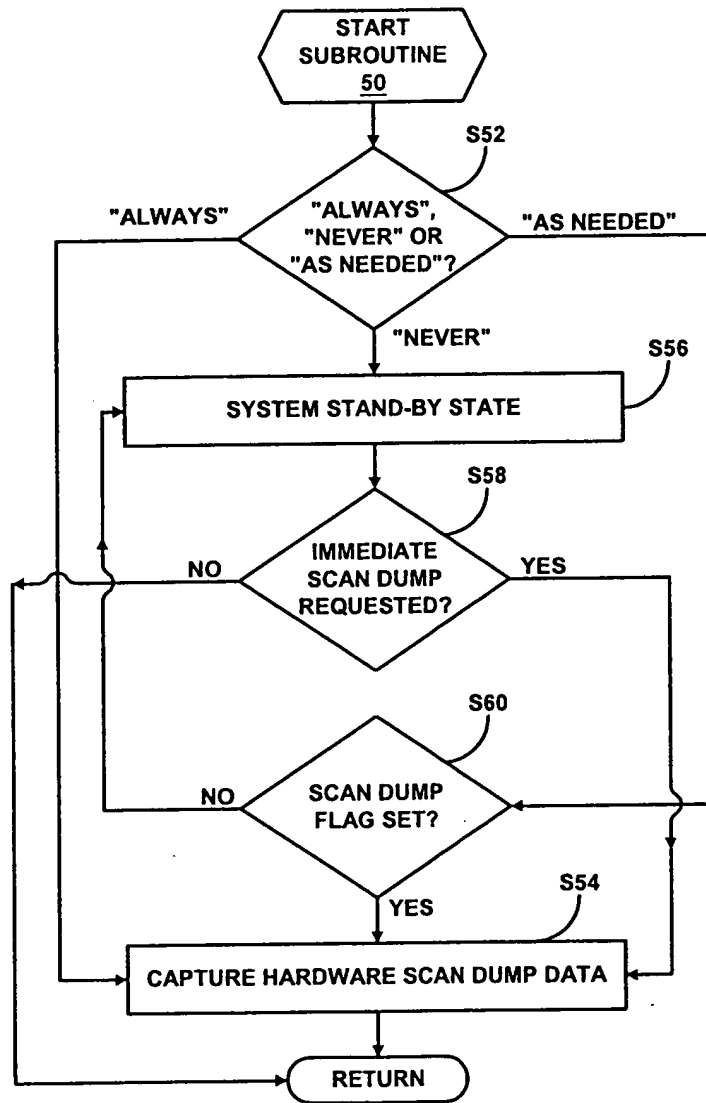


FIG. 4
4/5
AUS9-2001-0128-US1

70

ERROR SUBCLASS	ERROR DESCRIPTION	BIT OF ERROR DATA SIGNAL
CLASS 2A	HARDWARE HANG/HANG RECOVERY FAILURE	20 (SET STATE)
CLASS 2B	HARDWARE DESIGN	21 (SET STATE)
CLASS 2C	SOFTWARE/FIRMWARE DESIGN	22 (SET STATE)
CLASS 2D	SOFTWARE/FIRMWARE ILLEGAL OPERATION	23 (SET STATE)
CLASS 2E	INVALID ERROR CONDITIONS	24 (SET STATE)

FIG. 5
5/5
AUS9-2001-0128-US1

FIG. 5